Ultrathin Body InGaAs MOSFETs on III-V-On-Insulator Integrated With Silicon Active Substrate (III-V-OIAS)

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***Abstract*— Thin-body self-aligned InGaAs MOSFETs are fabricated on a III-V-On-Insulator structure on a silicon active substrate (III-V-OIAS). The p-type Si active substrate acts as a back gate that can modulate the threshold voltage and other electrical characteristics of the device. This paper explores the physics behind this effect through 2-D simulations and comparison with experiments. In the off-state, we find that the application of a positive body-to-source (V_{bs}) voltage increases the subthreshold swing but reduces drain-induced barrier lowering. The first effect is related to the electron profile and the location of the centroid of electron charge in the channel while the second is closely associated with the modulation of a depletion region in the silicon substrate. In the on-state, the series resistance is observed to improve under positive V_{bs} due to the increased accumulation of electrons in the extrinsic portion of the device. In addition, the channel mobility exhibits a two-branch behavior in its dependence on the average vertical electric field in the channel. This is explained by the different interfacial scattering that takes place at the front and back channel surfaces. This paper highlights the tradeoffs involved in attempting to exploit the body bias in the operation of QW-MOSFETs in III-V-On-Insulator with active substrate.**

***Index Terms*— III-V-On-Insulator, drain-induced barrier lowering (DIBL), mobility, quantum-well MOSFETs, subthreshold swing.**

I. Introduction

InAs-RICH InGaAs is a promising channel material for future CMOS applications due to its superior electron transport properties [1]–[4]. Tremendous progress has recently been made in III-V MOSFET research, including advances in performance and 3-D device architectures suitable for scaling [5]–[7]. This has brought to the fore the need for developing effective integration strategies of III-V MOSFETs onto a Si substrate.

An emerging integration scheme is via the use of wafer bonding to produce a III-V-On-Insulator substrate [8]–[12]. Ultrathin-body InGaAs MOSFETs built on such a platform incorporate a buried body terminal [13]. This allows the use of the substrate as a back gate of the transistors. By applying a back gate voltage, the threshold voltage can be modulated. Such dynamic threshold voltage control can be instrumental in achieving energy-efficient high-performance computing as well as ultralow-power applications. In Si, the same effect has been exploited for some time as the so-called silicon-on-insulator with active substrate (SOIAS) technology [14], [15]. While fairly well understood in the case of Si MOSFETs, the relevant device design and operation of III-V MOSFETs integrated on a silicon active substrate, or III-V-OIAS, has received little attention to date.

This paper builds on our recent demonstration of self-aligned InGaAs MOSFETs on SOI-like substrate, where, for the first time, we observed a strong impact of the back gate bias (V_{bs}) on various device figures of merit [13]. The threshold voltage (V_t), parasitic series resistance (R_{sd}), drain-induced barrier lowering (DIBL), subthreshold swing (S), and long-channel effective mobility (μ_{eff}) all exhibit a strong dependence on V_{bs}. In this paper, we study the physical origin of this device behavior through 2-D simulations. Understanding this should be instrumental in more effective device design as well as provide ideas for use at circuit level.

II. III-V-OIAS MOSFETs

A cross-sectional schematic of the InGaAs MOSFET on III-V-SOIAS studied here is shown in Fig. 1(a). A TEM cross section of a fabricated device with a gate length of 50 nm is shown in Fig. 1(b). The key steps in the fabrication of these devices are illustrated in Fig. 2.

Substrate fabrication follows the method described in [16]. The III-V heterostructure is first grown by MBE on a semi-insulating InP donor wafer. The growth order is inverse from how it appears in Fig. 1(a). Starting from an InP donor wafer substrate [see Fig. 2(a)], the layer structure consists of an InGaAs/InAlAs sacrificial etch-stop bilayer

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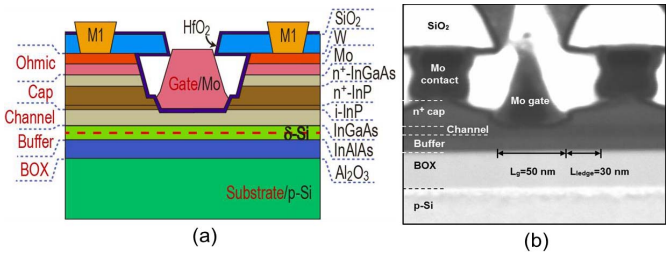

Fig. 1. (a) Cross-sectional schematic of InGaAs MOSFET on III-V-O-I with active silicon substrate. (b) TEM cross-sectional view of a fabricated MOSFET with a gate length of 50 nm and a ledge length of 30 nm.

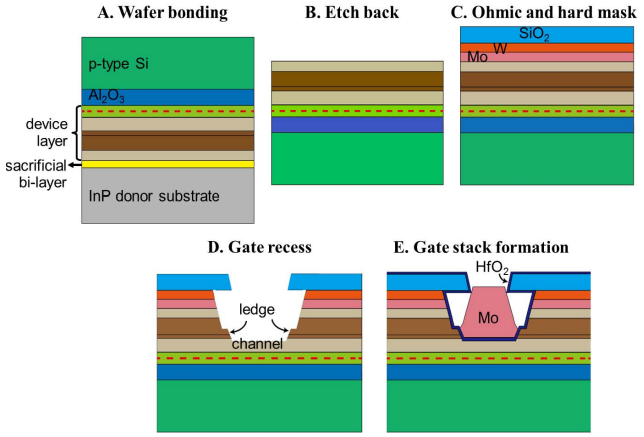

Fig. 2. Schematic of key steps of the fabrication process of InGaAs MOSFETs on III-V-OIAS. (a) Wafer bonding. (b) Etch back. (c) Ohmic and hard mask. (d) Gate recess. (e) Gate stack formation.

followed by two highly doped n^+ capping layers (23 nm in total), a not-intentionally-doped InP etch stopper (3 nm), a strained $In_{0.7}Ga_{0.3}As$ channel (10 nm), a thin InAlAs buffer layer (10 nm), and a 1-nm InGaAs protection layer. This top thin InGaAs layer later serves as interface to the buried oxide (BOX) and becomes fully oxidized. Little influence on device operation is expected from such a thin layer, so it is not included in the schematic nor the simulations. A Si δ-doped sheet with $N_s = 1 \times 10^{12}$ cm^{-2} is located inside the InAlAs buffer layer at a distance of 5 nm away from the channel.

Substrate fabrication continues the deposition of a 30-nm-thick Al_2O_3 BOX layer by ALD. The wafer is then bonded to a p-type Si wafer with a doping concentration of 1×10^{17} cm^{-3}, which was previously treated to form a thin hydrophilic chemically grown oxide on the surface. This is step A in the fabrication sequence illustrated in Fig. 2.

Following this, the InP donor wafer is wet etched down to the InGaAs/InAlAs etch-stop bilayer to release the device heterostructure on the Si wafer. A final selective chemical etch back is utilized to eliminate the InGaAs/InAlAs etch-stop bilayer and expose the n^+ InGaAs layer (step B). The resulting surface roughness at this point is RMS = 0.25 nm, almost identical to that of an as-grown substrate.

Device fabrication follows the self-aligned tight-pitch process described in [17]. This device architecture incorporates a thin highly conductive n^+-InP ledge spanning the access region of the device, as shown in Fig. 1. The role of the ledge is to reduce access resistance to the intrinsic portion of the device. The first step in the device fabrication process is ohmic metal (Mo/W bilayer) sputtering followed by hard mask (SiO_2) CVD deposition (step C). The gate region is then patterned using E-beam lithography, followed by a novel gate recess procedure that is based on RIE and digital etch, as described in [17]. Our recess approach allows precise control of three critical device dimensions: 1) channel thickness; 2) ledge length; and 3) ledge thickness (step D). The recess depth is calibrated so that the final device is a surface-channel MOSFET with an 8-nm-thick $In_{0.7}Ga_{0.3}As$ channel. The ledge thickness is about 20 nm and the ledge length is 30 nm.

Immediately after the last digital etch cycle, 3.5 nm of HfO_2 (EOT = 0.7 nm) is deposited by ALD as gate dielectric, followed by Mo evaporation and gate definition (step E). Finally, contact vias are opened through the oxide and a Ti/Au bilayer is evaporated and lifted off to form the contact pads, as shown in Fig. 1(a).

Our process is designed to emphasize CMOS fabrication compatibility. The front-end process is wet-etch free (no bulk semiconductor removal by wet process), lift-off free, and Au-free. As the cross-sectional TEM in Fig. 1(b) shows, we demonstrate 150-nm ohmic contact pitch with 50-nm gate length III-V MOSFETs.

III. Electrical Characteristics

The output I_d–V_{ds} characteristics of a transistor with $L_g = 70$ nm are shown in Fig. 3(a)–(c) for V_{bs} at −2, 0, and 3 V. The device drive current, under the same gate overdrive condition, increases as V_{bs} is made more positive. The transconductance is also increased under positive V_{bs}. For negative V_{bs}, the output characteristics show a noticeable increase in output conductance when $V_{ds} > 0.4$ V.

The subthreshold I_d–V_{gs} characteristics for $V_{ds} = 0.05$ and 0.5 V are shown in Fig. 4 for the same device as in Fig. 3 at the same three values of V_{bs}. An attractive feature of the III-V-OIAS technology is that V_{bs} shifts the V_t of the device, increasing V_t for decreasing V_{bs}. For negative V_{bs}, V_t shift and the sharpening of S combine to yield an extremely small OFF-state current. At $V_{bs} = -2$ V and $V_{ds} = 0.5$ V, an OFF-state current of 0.26 nA/μm is measured at $V_{gs} = -0.4$ V. For this device at $V_{gs} = -0.4$ V, $V_{ds} = 0$, the front gate leakage is very low: $I_g = 0.1$ m. Fig. 5 shows the evolution of the minimum subthreshold swing (S_{min}) of the 70 nm device as a function of V_{bs} at a drain bias of 0.5 V. At $V_{bs} = -2$ V, an S_{min} of 128 mV/dec and a DIBL of 209 mV/V are obtained. S increases and DIBL decreases, as V_{bs} becomes more positive.

In order to further our understanding, we have also characterized devices with a wide range of gate lengths, from $L_g = 70$ nm to $L_g = 1$ μm. For those devices, DIBL is measured at the constant current level where the steepest subthreshold swing is obtained. As noted, DIBL and S exhibit opposite trends with respect to V_{bs}. As shown in Fig. 6, DIBL decreases from a value of 270 mV/V at negative V_{bs} to about 120 mV/V at positive V_{bs} for $L_g = 70$ nm. A similar trend is observed in a long-channel device ($L_g = 1$ μm) but

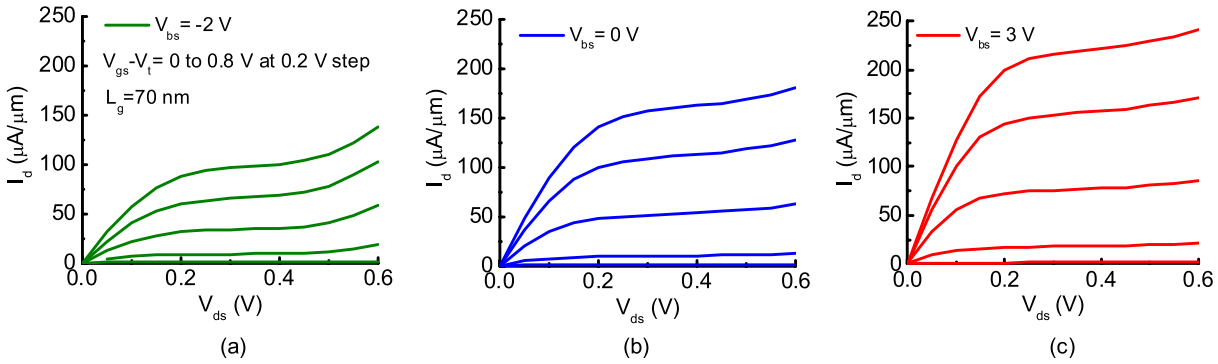

Fig. 3. Output characteristics of an InGaAs MOSFET with a gate length of 70 nm at $V_{\rm bs} = -2$, 0, and 3 V (from left to right).

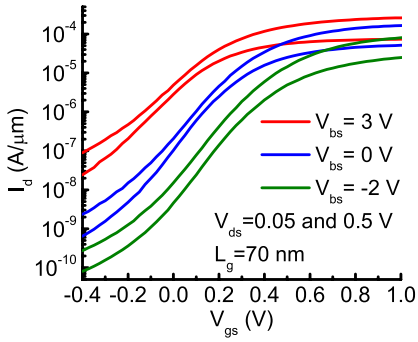

Fig. 4. Subthreshold characteristics of InGaAs MOSFET with a gate length of 70 nm at $V_{\rm bs} = -2$, 0, and 3 V.

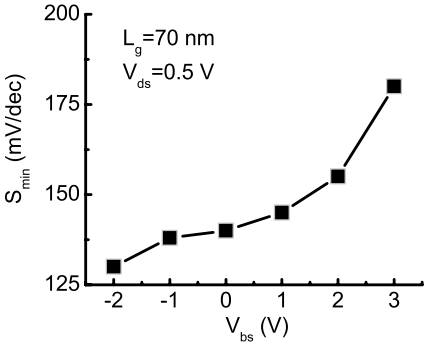

Fig. 5. Minimum subthreshold swing at $V_{\rm ds} = 0.5$ V versus $V_{\rm bs}$ for InGaAs MOSFET with $L_g = 70$ nm.

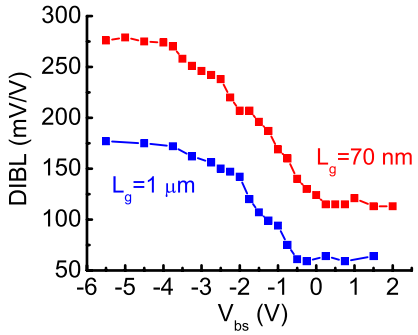

Fig. 6. DIBL versus $V_{\rm bs}$ for InGaAs MOSFETs with $L_g = 70$ nm and 1 μm.

with smaller overall DIBL values. The physical origin for this behavior will be discussed in Sec. IV.

Low static leakage is important for low-power applications. Static leakage includes currents through the front gate and

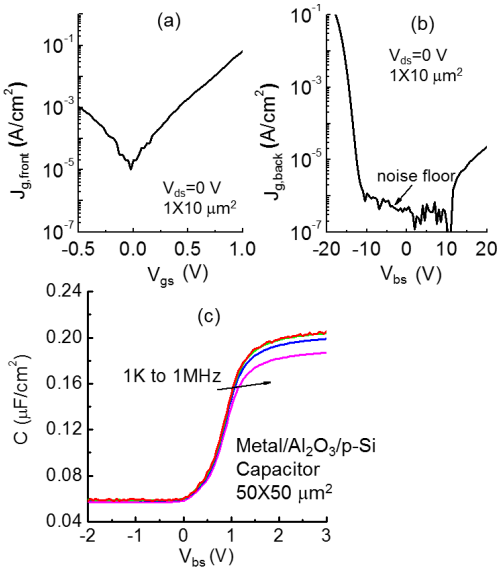

Fig. 7. (a) Front gate current leakage ($V_{\rm bs} = 0$ V, $V_{\rm ds} = 0$ V). (b) Leakage through the back gate capacitor ($V_{\rm gs} = 0$ V, $V_{\rm ds} = 0$ V). (c) C–V of the back gate capacitor.

the BOX, as well as the direct drain-to-source current. In our device, the leakage current densities through the front gate and the BOX are much lower than the source-to-drain leakage. Fig. 7(a) shows the front gate current density measured by sweeping $V_{\rm gs}$ at the front gate and grounding S/D in a long-channel MOSFET. $V_{\rm bs}$ is at 0 V for this measurement. Within a $V_{\rm gs}$ span of -0.5 to 0.5 V, the front gate current leakage is below 2×10^{-3} A/cm^2.

In order to gain a better understanding of the quality of BOX MOS structure, we fabricated a separate BOX capacitor with a metal/Al_2O_3(BOX)/p-Si structure. The leakage through this capacitor is shown in Fig. 7(b). The device area is 100×100 μm^2. Leakage is below the detection limit of the measurement system up to ± 10 V. This clearly indicates that current leakage through the BOX in our MOSFETs is negligible. $V_{\rm gs}$ is at 0 V for this measurement.

Fig. 7(c) shows C–V measurements of the BOX/p-silicon capacitor. High-quality characteristics are obtained with small frequency dispersion and negligible hysteresis (not shown). The flatband voltage of this MOS capacitor is about 0 V.

Fig. 8(a) shows $V_{t,\rm sat}$ of a long-channel MOSFET ($L_g = 1$ μm) against $V_{\rm bs}$. $V_{t,\rm sat}$is the threshold voltage

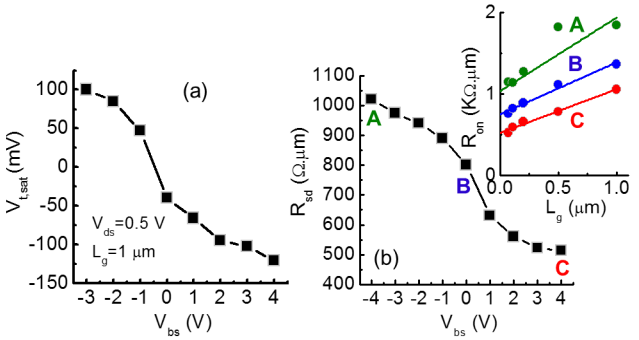

Fig. 8. (a) V_t at $V_{ds} = 0.5$ V versus V_{bs} for a long-channel InGaAs MOSFET. (b) External parasitic R_{sd} at varying V_{bs}. Insets: extraction of R_{sd} from measurements of R_{on} as a function of L_g for different values of V_{bs}.

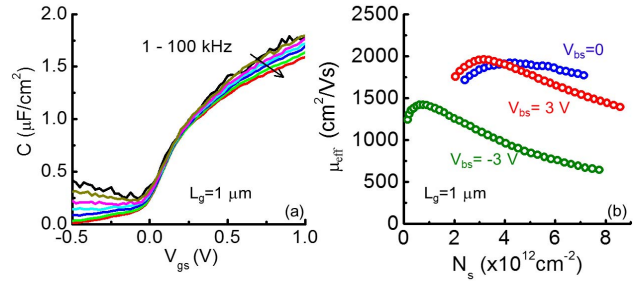

Fig. 9. (a) Split C–V measurements at $V_{bs} = 0$ V. (b) Effective field mobility in long-channel InGaAs MOSFET extracted by split C–V method versus channel carrier density at $V_{bs} = -3$, 0, and 3 V.

extracted at $V_{ds} = 0.5$ V at a drain current of 1 μA/μm. When V_{bs} changes from -3 to 4 V, $V_{t,sat}$ drops by 220 mV. ON-resistance measurements were also performed for devices with different gate lengths for different values of V_{gs} [inset of Fig. 8(b)]. From these, the parasitic resistance R_{sd} was extracted by extrapolation to $L_g = 0$. The result is shown in Fig. 8(b). R_{sd} is found to decrease in half when V_{bs} increases from -4 to 4 V.

We have also extracted the apparent electron mobility by the split-C–V method. Due to the long gate length, the impact of series resistance is negligible. Fig. 9(a) shows the split-C–V measurements at $V_{bs} = 0$ for various frequencies. The capacitance shows significant frequency dispersion at low frequency. This is believed to be the result of interface traps that respond at lower frequencies and the large RC time constant of the device when the channel is turned OFF. For reliable mobility extraction, the high-frequency (100 kHz) characteristics are used. At high gate overdrive, when the channel charge becomes dominant, this should give good confidence on the electron mobility extraction. In this regime, in fact, Fig. 9(b) shows that there is significant degradation of mobility for negative V_{bs}.

We summarize the impact of substrate bias on device electrical characteristics in Table I.

IV. Device Modeling

In order to understand the above experimental results, we have carried out 2-D Poisson–Schrödinger simulations using Nextnano [18] and 2-D Poisson–Boltzmann (classical) simulations using Sentaurus Device [19].

TABLE I

Summary of Device Electrical Characteristics for Positive and Negative V_{bs} Respectively

	Positive V_{bs}	Negative V_{bs}
DIBL	Decrease	Increase
Subthreshold swing	Increase	Decrease
Off state leakage	Increase	Decrease
Output conductance	Decrease	Increase
R_{sd}	Decrease	Increase
Mobility	Increase	Decrease
Transconductance	Increase	Decrease
Threshold voltage	Decrease	Increase

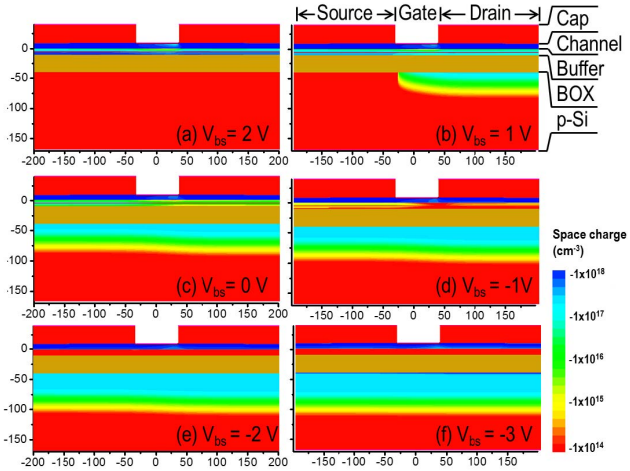

Fig. 10. Classical electrostatic simulations of the InGaAs MOSFET on p-type silicon substrate ($N_A = 10^{17}$ cm^{-3}). (a)–(f) Space charge contours for V_{bs} from 2 to -3 V, respectively, V_{bs} step being -1 V. V_{ds} is at 0.5 V and gate overdrive is 0.1 V. The color scale on the right indicates the space charge with blue region for being large in magnitude and red region for small.

Simulations of the electrostatics of an InGaAs MOSFET on III-V-OIAS in the ON state, as obtained by Sentaurus Device, are shown in Fig. 10 for $V_{gs} - V_t = 0.1$ V, $V_{ds} = 0.5$ V, and different values of V_{bs}. The gate length is 70 nm. For high positive V_{bs}, there is virtually no space-charge region (SCR) in the silicon substrate. At $V_{bs} = 1$ V, an SCR is formed in the substrate surface under the drain and the gate but not under the source. As V_{bs} becomes more negative, the SCR first spreads under the source and then it continues to grow vertically until substrate inversion happens at around $V_{bs} = -3$ V [Fig. 10(f)]. The appearance of an SCR at the substrate surface for negative V_{bs} results in poor electrostatic isolation between the drain and the channel. This is postulated to be the origin for degraded DIBL at negative V_{bs}.

At negative V_{bs}, the large DIBL for long-channel transistor, even at $L_g = 1$ μm, is due to the formation of the depletion and inversion layer. The floating depletion and inversion layer beneath the BOX couples the drain potential to the channel.

Further insight into the role of substrate bias on device characteristics can be obtained from studying the charge distribution in the quantum-well channel. For this, 2-D Poisson–Schrödinger simulations are performed. In these simulations, parabolic bands are assumed with an isotropic effective mass for $In_{0.7}Ga_{0.3}As$ of $m_e^* = 0.036$ m_0.

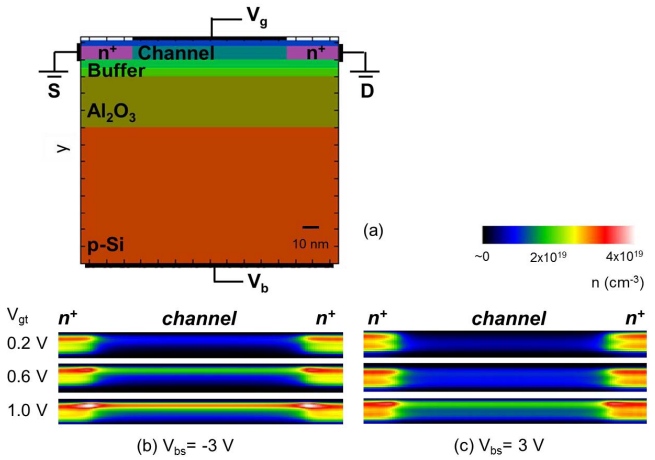

Fig. 11. 2-D Poisson–Schrödinger simulations of a prototypical InGaAs MOSFET on insulator. (a) Simulated structure. The gate length is 90 nm. The n^+ S/D regions are assumed to be directly connected to the channel at the gate edge. Only equilibrium condition ($V_{ds} = 0$ V) is considered so drain and source are both connected to ground. The simulated 2-D electron concentration profile in the quantum well channel for (b) $V_{bs} = -3$ V and (c) $V_{bs} = 3$ V at given gate overdrives.

A schematic of the simulated device structure is shown in Fig. 11(a). For simplicity, it is assumed that the n^+ InGaAs source and drain channel-contact regions (set to ground) are placed right next to the gate edge. The bottom boundary assumes a contact that can modulate the potential of the silicon substrate. The bulk silicon is thick enough to make sure a quasi-neutral region with zero electric field extends sufficiently below the device. The Poisson–Schrödinger equations are only solved in a limited region: from the gate dielectric to the top interface of the BOX. The other regions are treated classically.

Fig. 11(b) and (c) shows the simulated electron density distribution at $V_{bs} = -3$ V and $V_{bs} = 3$ V with a gate overdrive of 0.2, 0.6, and 1 V, respectively. Under negative V_{bs}, electrons first populate the channel at its top. However, under positive V_{bs}, electrons first appear toward the bottom of the channel, with the centroid of charge moving gradually toward the top as V_{gs} increases. For $V_{bs} = -3$ V and $V_{gt} = 1$ V, the electron concentration is rather peaky at the top while for $V_{bs} = 3$ V, the electron distribution is broader across the channel.

The evolution of the electrostatics as V_{bs} changes can be best seen by examining the energy band diagram (E_c) in the transverse direction at the center of the device. This is shown in Fig. 12 for $V_{gs} = 0$ V at different values of V_{bs}. Fig. 12(b) is an enlarged view of the same plot around the channel region.

At negative V_{bs}, the Fermi level is pulled up in the silicon substrate with respect to the gate and S/D. This brings up the conduction band in the channel and effectively shifts V_t positive. For positive V_{bs}, the contrary happens.

To explore the impact of this, Fig. 13 depicts the simulated sheet electron density (N_s) in the channel against V_{gs}. Indeed, the simulated V_t shift of the device agrees with the trend in Fig. 8(a). The saturation of the experimental V_t shift for large positive and negative values of V_{bs} is most likely the result of interface states in the front and back channel interfaces which are not included in the model.

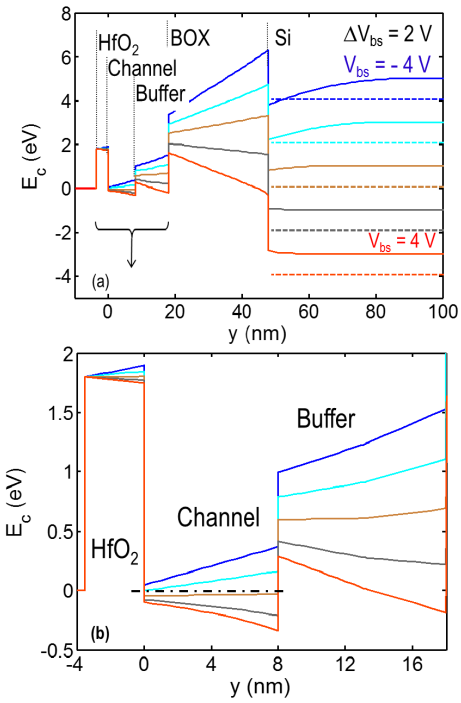

Fig. 12. (a) Conduction band diagram from metal to the silicon substrate along a vertical path at the center of the simulated structure in Fig. 11(a), the dashed line indicating the electron quasi-Fermi level in the silicon substrate. (b) Enlarged conduction band diagram in the channel region, the dashed-dotted line indicating the electron quasi-Fermi level in the channel.

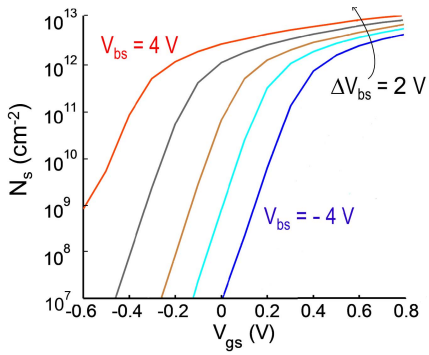

Fig. 13. Simulated sheet carrier density versus gate voltage from the Poisson–Schrödinger simulations.

The change in charge in the channel as a result of the application of V_{bs} also affects the access regions. This impacts on the access resistance. The application of negative V_{bs} reduces N_s and increases the parasitic resistance R_{sd}. The contrary happens for positive V_{bs}. This is consistent with the experimental observations of Fig. 8(b).

V_{bs} not only changes the integrated electron concentration in the channel but also affects the spatial electron distribution. This has important consequences. Fig. 14 plots three sets of energy band diagrams and electron concentration profiles in the channel for a V_{bs} of -2, 0, and 2 V. The gate bias is selected so that the same sheet electron density is present in the channel ($N_s = 4 \times 10^{12}$ cm^{-2}). Under this condition, the conduction band in the channel bends down toward the

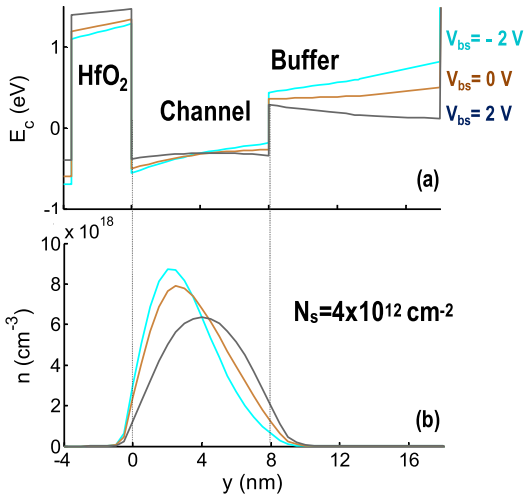

Fig. 14. At a fixed sheet carrier density of 4×10^{12} cm^{-2}, (a) band diagram and (b) charge distribution in the transverse direction for V_{bs} of -2, 0, and 2 V.

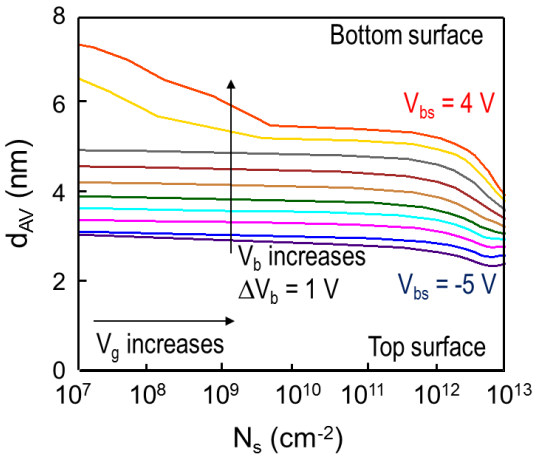

Fig. 15. Distance of the electron distribution centroid from the top channel surface d_{av}, versus sheet charge density N_s, in semilog scale for the subthreshold region at various V_{bs}. d_{av} generally decreases as N_s increases.

top at negative V_{bs}, while it is flatter for positive V_{bs}. Consequently, the centroid of the electron distribution in the channel is closer to the front gate under negative V_{gs} and it moves further away as V_{bs} is made more positive.

To quantitatively analyze this, we define d_{av}, the distance of the centroid of the carrier distribution from the HfO_2/InGaAs interface. Fig. 15 shows d_{av} versus N_s with N_s plotted in a log scale. As N_s increases with increasing gate overdrive, the centroid of charge moves toward the top of the channel. For a given N_s, increasingly negative V_{bs} brings the centroid of charge closer to the top interface while positive V_{bs} lowers the centroid of charge closer to the bottom of the channel. This is more prominent in the subthreshold regime, $N_s < 10^{10}$ cm^{-2}.

For very positive V_{bs} and low N_s, we see in Fig. 15 that the centroid of charge is initially inside the InAlAs buffer before eventually moving into the channel as N_s increases. This is consistent with our observation of a degradation of the subthreshold swing and higher OFF-state leakage observed in the experiments for positive V_{bs} (Fig. 4). This occurs as a result of the population of the InAlAs delta-doped layer with electrons and the poor gate efficiency when the centroid of charge is far away from the gate (see also Fig. 13).

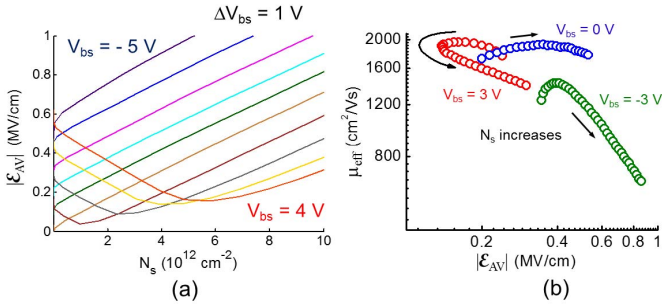

Fig. 16. (a) Average electric field in the channel versus sheet charge density for various V_{bs}. (b) Effective mobility versus $|\mathcal{E}_{AV}|$. The arrow indicates increasing sheet electron concentration in the channel.

V_{bs} also affects the vertical E-field that is experienced by the channel electrons, thus impacting on their mobility. It is well known that channel carriers follow the so-called universal mobility in bulk Si MOSFETs [20], where mobility is degraded at higher effective E-field ($\mathcal{E}_{eff}$). Our SOI-like transistors allow us to test this in the InGaAs MOS system. The calculation of $\mathcal{E}_{eff}$ in an SOI-like thin-body device requires some care. In [21] and [22], $\mathcal{E}_{eff}$ in an SOI or double gate device is defined as the weighted average of the magnitude of the local transverse electric field with the local carrier concentration. We can calculate $|\mathcal{E}_{AV}|$ in this manner from our QM simulations

$$|\mathcal{E}_{AV}| = \frac{\int |\mathcal{E}(y)| \cdot n(y) dy}{\int n(y) dy} \tag{1}$$

where $|\mathcal{E}(y)|$ is the local E-field magnitude defined by the local conduction band gradient. The resulting $|\mathcal{E}_{AV}|$ versus V_{gs} at different V_{bs} is shown in Fig. 16(a). Note that for positive V_{bs}, $|\mathcal{E}_{AV}|$ initially decreases as N_s increases, and then it starts increasing. This comes from the competing effect between front-gate and back-gate voltages. This is different from a bulk device where $|\mathcal{E}_{AV}|$ versus V_{gs} follows a monotonic trend and it is in agreement with a similar study of SOI MOSFETs [21].

In bulk InGaAs MOSFET under strong inversion condition, the effective mobility (μ_{eff}) exhibits a classic $|\mathcal{E}_{AV}|$ dependence [23], [24]. However, this needs not be the case in III-V-OIAS MOSFETs under applied back gate bias. We rearrange the mobility data in Fig. 9 and show μ_{eff} versus $|\mathcal{E}_{AV}|$ in Fig. 16(b) in a log-log scale. There appear to be two branches in the $\mu_{eff} - |\mathcal{E}_{AV}|$ dependence: An upper branch where the mobility is relatively high and exhibits a weak field dependence and a lower branch where mobility is lower and degrades quickly as the average field increases. A similar two-branch mobility phenomenon has been explored in SOI MOSFETs where the presence of two different gates results in a mobility that is dependent not only on the effective field but also on the particular carrier distribution [21]. In our case, the lower branch is associated with the front interface since it is mostly in action for negative values of V_{bs}. The upper branch is characterized by a lower effective field and greater exposure

to scattering at the remote back oxide/InAlAs interface that seems relatively more benign. This is not surprising since at the bottom of the channel there is a largely specular InGaAs/InAlAs interface and the oxide/InAlAs interface is relatively far away (∼10 nm). In contrast, at the top, there is a HfO_2/InGaAs interface directly on the channel.

We have successfully explained the trend observed in Table I by 2-D device models. One limitation of our models is not taking into account the effect of interface traps and bulk traps in the devices. These traps can be active in the dielectric and semiconductor layers. As a result, although the trends match, the values of experimental and model are not in total agreement. For example, the threshold voltage shift is more sensitive to $V_{\rm bs}$ change in the model than the experimental data indicate. This can be explained by the impact of interface traps and the resultant Fermi level pining at the back interface. Nevertheless, the relevant mechanisms pointed out in this work capture the essential physics.

V. Conclusion

In this paper, we demonstrate a III-V-OIAS technology that is promising for future low-power high-performance VLSI applications. An InGaAs MOSFET is integrated on a silicon active substrate through a wafer transfer process. By means of the back bias, the electrical characteristics of the device can be modulated in a manner that can be explained through 2-D device simulations. In particular, at negative $V_{\rm bs}$, the demonstrated III-V-OIAS technology offers a positive shift in V_t and a sharpening in subthreshold swing with no additional cost in static gate leakage. This offers the opportunity to efficiently reduce the static power consumption in VLSI circuits, making them attractive candidates in low-power applications.

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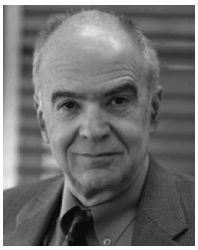

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